

**REMARKS**

Claims 1 through 9 remain pending in this application. In response to the Office Action, dated October 29, 2004, claims 1 through 5 and 7 through 9 have been amended. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application as amended is respectfully solicited.

Claims 1 through 9 have been rejected under the second paragraph of 35 U. S. C. § 112. Paragraph 3 of the Office Action identifies specific phrases in claims 1, 2 and 5 through 9 that were held to be confusing. In response, claims 1 through 5 and 7 through 9 have been amended to clarify the subject matter recited.

The present invention is based on a configuration in which one local sense amplifier is shared among a plurality of bit line pairs. In a hierarchical configuration, a local sense amplifier ( lower hierarchy sense amplifier) can select one pair from a plurality of bit line pairs to amplify the data, and a global sense amplifier (higher hierarchy sense amplifier) can select one of a plurality of such local sense amplifiers to amplify data. Complementary signal lines are connected between the memory cell bit lines and a lower hierarchy sense amplifier and other complementary signal lines are connected between the lower hierarchy sense amplifiers and the higher hierarchy sense amplifier(s). The claim amendments clarify the specific relationships among memory cell, bit lines, complementary signal lines and lower and higher hierarchy sense amplifiers. With respect to claim 5, the recited transmission gate corresponds, for example, to the lower hierarchy sense amplifier structure illustrated in Fig. 14, described at page 16 of the specification.

It is believed that claims 1 through 9 as now amended fully clarifies the invention within the requirements of the second paragraph of 35 U. S. C. § 112. Withdrawal of the rejection is respectfully solicited.

Claims 1 through 5 have been rejected under 35 U. S. C. § 102(b) as being anticipated by U.S. patent 5,724,292 (Wada). The rejection is stated at paragraph 5 of the Office Action. Claims 6 through 9 have been rejected under 35 U. S. C. § 103 as being unpatentable over Wada in view of U.S. published application 2004/0022109 (Yoon), as set forth at paragraph 7 of the Office Action. Yoon has been relied upon for concluding that the additional recitations of the dependent claims would have been obvious modifications of the Wada arrangement. Reconsideration of the rejections in light of the amendments to the claims and the following comments is respectfully solicited.

Wada is directed to an SRAM that allows destructive readout to reduce the memory cell area. In order to restore data that has been destroyed after readout, a sense amplifier (100 in Fig. 1) is prepared for each bit line pair. Following data input in the sense amplifier, one bit line is driven to the power supply level and the other bit line is driven to the GND level in accordance with the input data in the same cycle. Therefore, the sense amplifier is still connected to the bit line when the sense amplifier is driven.

The present invention provides a reduction of the potential amplitude of the bit line. Therefore, the present invention is configured such that the sense amplifier is electrically disconnected from the bit line pair when the local sense amplifier (SA1 of Fig. 1) is driven. It is not necessary to prepare a local sense amplifier for each bit line pair. The present invention is based on a configuration in which one local sense amplifier is shared among a plurality of bit line pairs. Independent claim 1 has been amended to expressly recite, *inter alia*, the following:

wherein, when a sense amplifier of higher hierarchy level of said sense amplifier group is active, said active sense amplifier has no electrical interconnection with the complementary signal lines of said complementary signal line group for connecting said active sense amplifier with the sense amplifier of lower hierarchy level of said sense amplifier group or said memory cell.

Although Wada shows a second sense amplifier (PREAMP of Fig. 1) and seems to have a hierarchical structure, the second sense amplifier is not necessarily required since the potential difference of the bit line pair is amplified sufficiently through the sense amplifier, as described above. Wada is silent about the operation timing thereof. The semiconductor memory device of Wada employs a two-stage sense amplifier scheme, rather than a hierarchy.

In the invention of the subject application, the output potential of the local sense amplifier must be amplified by a global sense amplifier (HSA of Fig. 1) since the output potential of the local sense amplifier is small. In order to keep the potential difference of the global bit lines (HBT, HBTC) small, the present invention is configured to have the sense amplifier electrically disconnected from the global bit line pair (by signal HSE) at the same moment of operation of the global sense amplifier. This feature has now been specifically recited in claim 1. Thus, a hierarchical configuration includes a local sense amplifier selecting one pair from a plurality of bit line pairs to amplify the data, and a global sense amplifier selecting one of the plurality of local sense amplifiers to amplify data.

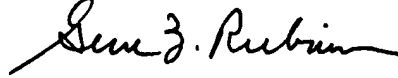
It is submitted that neither Wada nor Yoon teaches the claimed hierarchical arrangement with respective sense amplifiers disconnected from the signal line. Accordingly, withdrawal of the rejections and allowance of the application are respectively solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please

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Respectfully submitted,

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